REMARKS

Claims 1-23 are now present in this application.

Claim 18 has been amended, and claim 23 has been presented. Reconsideration of the application, as amended, is respectfully requested.

The drawings stand objected to under 37 CFR 1.83(a). The Examiner has asserted that a fourth NMOS component and a fifth NMOS component, connected in series between the pad and I/O low power line, is not shown in the drawings. It is respectfully submitted, however, that this feature is shown in Fig. 14. Accordingly, reconsideration and withdrawal of any objection to the drawings are respectfully requested.

Claim 18 stands objected to for an informality. In view of the foregoing amendments, it is respectfully submitted that this informality has been addressed. Reconsideration and withdrawal of any objection to the claims are respectfully requested.

Claim 21 stands rejected under 35 USC 112, second paragraph. This rejection is respectfully traversed.

In view of the foregoing amendments and remarks, it is respectfully submitted that claim 21 particularly points out and distinctly claims the subject matter of the instant invention. Accordingly, reconsideration and withdrawal of the 35 USC 112, second paragraph rejection are respectfully requested.

Claims 1, 4-6, 8-12, 15 and 16 stand rejected under 35 USC 102(b) as being anticipated by PUAR, U.S. Patent 5,287,241. This rejection is respectfully traversed.

Claim 2 stands rejected under 35 USC 103 as being unpatentable over PUAR in view of POPLEVINE et al., U.S. Patent 6,184,557. This rejection is respectfully traversed.

Claims 7, 13 and 14 stand rejected under 35 USC 103 as being unpatentable over PUAR in view of WATT, U.S. Patent 5,477,413. This rejection is respectfully traversed.

Claim 17 stands rejected under 35 USC 103 as being unpatentable over PUAR in view of MALONEY, U.S. Patent 5,530,612. This rejection is respectfully traversed.

Claims 18 and 22 stand rejected under 35 USC 103 as being unpatentable over PUAR in view of ADAMS et al., U.S. Patent 4,782,250, and further in view of WAGGONER, U.S. Patent 5,917,220. This rejection is respectfully traversed.

Claim 21 stands rejected under 35 USC 103 as being unpatentable over PUAR in view of ADAMS et al. and WAGGONER, and further in view of WATT. This rejection is respectfully traversed.

35 USC 102(b) Rejections

Regarding claim 1, the Examiner asserts that PUAR discloses all the elements of claim 1, for example, the p-type drain and the first well in claim 1. However, the p-type doped region is, in

fact, the drain of the PMOS transistor P2. Accordingly, one of ordinary skill in the art would not read a drain region of a MOS as a well region, due to different doped concentration, process sequence, and other factors. Accordingly, the p-type drain of the MOS transistor P2 is not identical to the first well as claimed in claim 1, and thus, PUAR does not disclose all the features of independent claim 1. Accordingly, it is respectfully submitted that independent claim 1, as well as its dependent claims 2, 4-6 and 8, are neither taught nor suggested by the prior art utilized by the Examiner.

Regarding claim 4, the Examiner asserts that the p-type drain and the first well in claim 1 are rear on, as are the NMOS transistor N2 and the claimed functional component. In claim 4, the functional component comprises a MOS transistor having the second conductivity type **in the first well**. The NMOS transistor N2 in PUAR, however, is not in the p-type drain. PUAR therefore does not disclose all of the features of claim 4. Accordingly, it is respectfully submitted that claim 4 is neither taught nor suggested by the prior art utilized by the Examiner.

Regarding claims 9 and 15, the MOS component having a second conductivity type are formed in **a first well on the substrate and coupled to the pad, and an isolating region having a second conductivity type is formed between the first well and the substrate to separate the first well and the substrate**. In PUAR,

however, the NMOS transistor N2 is not formed in the p-type drain. Accordingly, PUAR does not disclose all of the features of claims 9 and 15. Accordingly, it is respectfully submitted that claims 9 and 15, as well as their dependent claims 10-12 and 16, are neither taught nor suggested by the prior art utilized by the Examiner.

Reconsideration and withdrawal of the 35 USC 102(b) rejections are therefore respectfully requested.

35 USC 103 Rejection

The Examiner is reminded that, to establish a prima facie case of obviousness, three criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teaching. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

Regarding claim 2, the Examiner asserts that it would have been obvious to one of ordinary skill in the art to have modified the PUAR solution by adding the second well and deep well according to POPLEVINE et al. because, as POPLEVINE et al. states, such a structure would provide more balanced capacitances and resistances and therefore, more symmetric outputs. The p-type doped region in PUAR, however, is the drain of the PMOS transistor P2, and thus,

one of ordinary skill in the art would not read the drain as the first well as claimed in claim 1. Accordingly, the p-type drain of the MOS transistor P2 is not identical to the first well as claimed in claim 1. Furthermore, in the present invention, the isolating well is provided to isolate the first well and the substrate such that the substantial amount of electrostatic charges isolated by the isolating well are discharged through the ESD clamp circuit to the pad, not through the functional component during an ESD event. The object is different from that stated in POPLEVINE et al. Therefore, there is no teaching or suggest to generate the claimed combination and the reasonable expectation of success in PUAR and POPLEVINE et al. Moreover, one of ordinary skill in the art would have no motivation to combine PUAR and POPLEVINE et al. to obtain the claimed invention. Accordingly, it is respectfully submitted that claim 2 is neither taught nor suggested by the prior art utilized by the Examiner.

Regarding claim 7, the Examiner asserts that the p-type drain in PUAR and the first well in claim 1 are read on. The p-type doped region, however, is the drain o the PMOS transistor P2 and thus, persons in the art would not read a drain region of a MOS as a well region. Accordingly, the p-type drain of the MOS transistor P2 is not identical to the first well as claimed in claim 1. Accordingly, PUAR does not disclose all features of claim 1. Neither PUAR nor WATT teaches the first well on the substrate as recited in claim 1,

it is respectfully submitted that that claim 7 is neither taught nor suggested by the prior art utilized by the Examiner.

Regarding claims 13, 14, and 17, the MOS component having a second conductivity type is formed in a first well on the substrate and coupled to the pad, and an isolating region having a second conductivity type is formed between the first well and the substrate to separate the first well and the substrate. The NMOS transistor N2 in PUAR, however, is not in the p-type drain when the Examiner asserts that the drain and the first well are read on, and thus, PUAR does not disclose all of the features of independent claims 9 and 15, from which claims 13, 14 and 17 depend.

The secondary references utilized by the Examiner fail to overcome the deficiencies of the primary reference.

As neither PUAR, WATT, nor MALONEY teaches **a MOS component of a second conductivity type in the first well on the substrate**, as recited in claims 9 and 15, it is respectfully submitted that independent claims 9 and 15, from which claims 13, 14 and 17 depend, are neither taught nor suggested by the prior art utilized by the Examiner.

Regarding claims 18, 21 and 22, the MOS component having a second conductivity type is formed in a first well on the substrate and coupled to the pad, and an isolating region having a second conductivity type is formed between the first well and the substrate to separate the first well and the substrate. Further,

the second and third NMOS components are respectively formed in a P-type second isolated well on the substrate and connected in series, and an N-type second isolating region is formed between the P-type second isolated well and the substrate. The p-type doped region in PUAR, however, is the drain of the PMOS transistor P2 and, thus, one of ordinary skill in the art would not read the drain as the first well as claimed in claim 18. Further, one of ordinary skill in the art would have no motivation to dispose MOS components in a drain of another MOS component to obtain the claimed invention, when the Examiner asserts that the drain of the PMOS P2 and the first well are read on. Thus, there is no teaching or suggestion to generate the claimed combination and the reasonable expectation of success in PUAR, ADAMS et al., WAGGONER, and WATT. Accordingly, it is respectfully submitted that independent claim 18, as well as its dependent claims 21 and 22, are neither taught nor suggested by the prior art utilized by the Examiner.

Reconsideration and withdrawal of the 35 USC 103 rejections are therefore respectfully requested.

Applicants gratefully acknowledge that the Examiner considers claims 3, 19 and 20 to contain allowable subject matter. However, in view of the foregoing amendments and remarks, it is respectfully submitted that all claims should now be in condition for allowance.

Reconsideration and withdrawal of all objections and rejections are respectfully requested.

Favorable reconsideration and an early Notice of Allowance are earnestly solicited.

Because the additional prior art cited by the Examiner has been included merely to show the state of the prior art and has not been utilized to reject the claims, no further comments concerning these documents are considered necessary at this time.

In the event that any outstanding matters remain in this application, the Examiner is invited to contact the undersigned at (703) 205-8000 in the Washington, D.C. area.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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